



# SUMP Logic Analyzer

Analyseur logique sur base FPGA

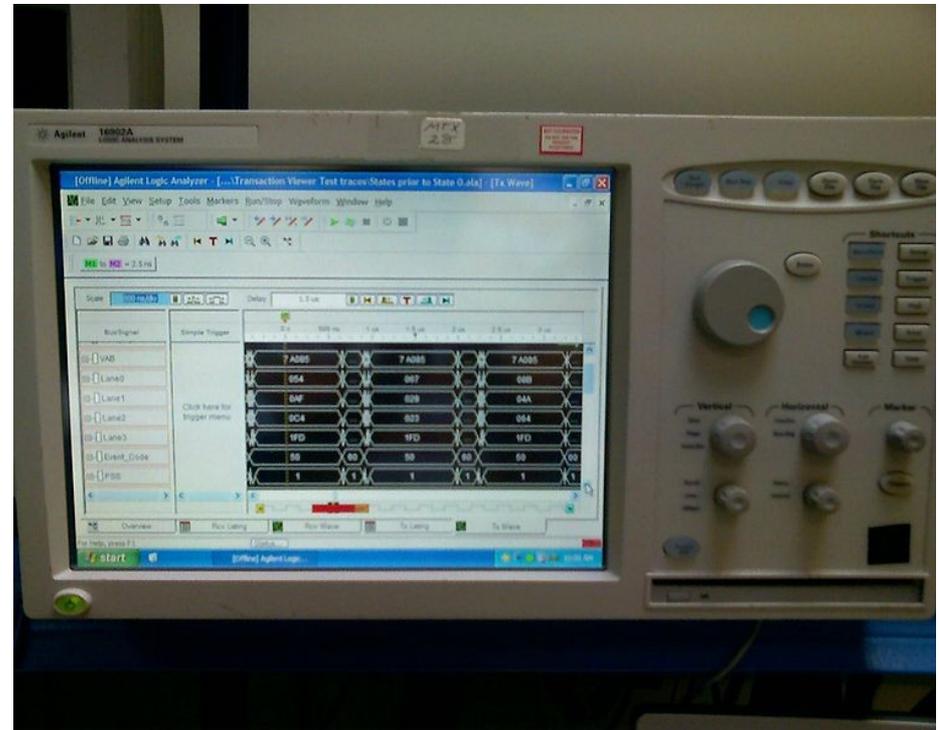
Etude de l'Amiga 500

# Analyseur Logique

- Qu'est-ce que c'est ?
- A quoi ça sert ?
- Caractéristiques
  - Nombre de voies
  - Fréquence
  - Mémoire
  - Triggers
  - Logiciel
- Modèles

# Analyseur Logique

- Actuels
  - Avantages
    - Puissance
    - Exploitation
  - Inconvénients
    - Prix
    - Encombrement



# Analyseur Logique

- Anciens
  - Avantages
    - Rapport qualité/prix
    - Puissance
  - Inconvénients
    - Approvisionnement
    - Encombrement
    - Exploitation



# Analyseur Logique

- USB
  - Avantages
    - Prix
    - Exploitation
    - Encombrement
  - Inconvénients
    - Puissance



# Analyseur Logique

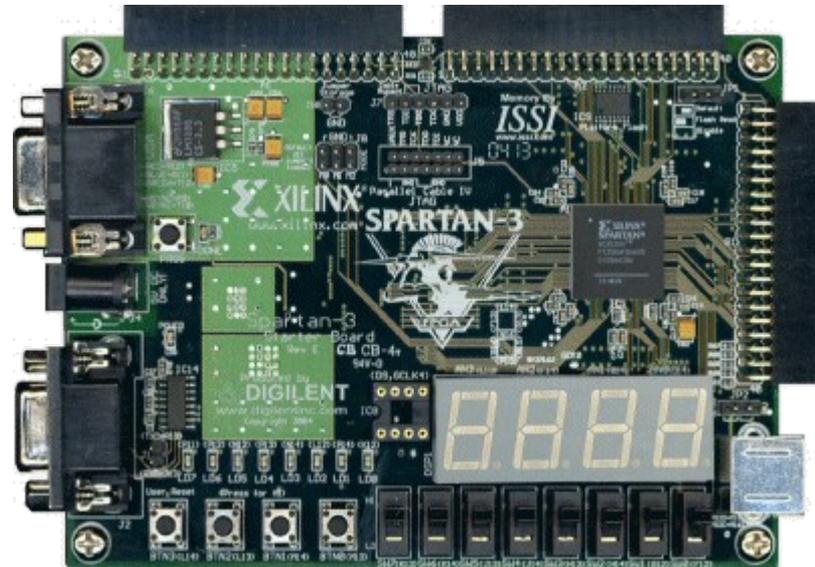
- SUMP Logic Analyzer

- Avantages

- Prix
    - Exploitation
    - Encombrement
    - Puissance
    - Autres utilisations

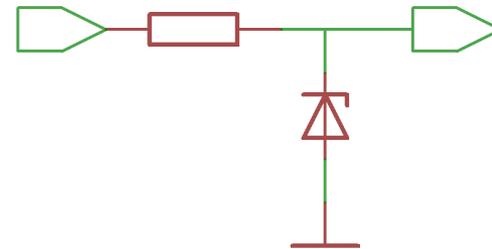
- Inconvénients

- Amateur



# SUMP Logic Analyzer

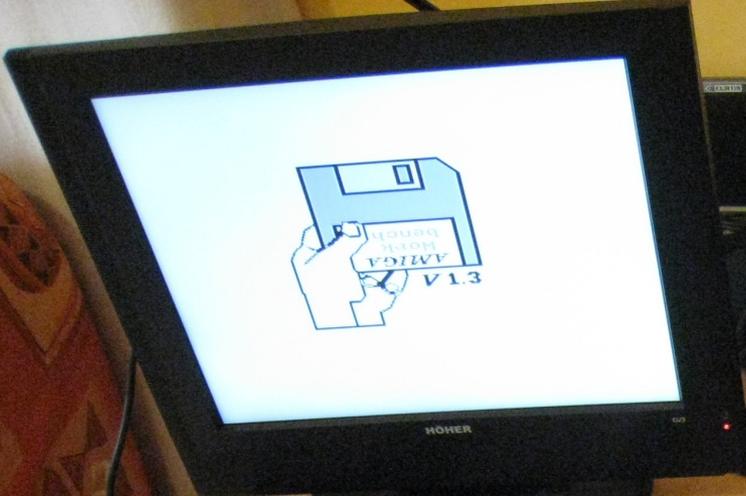
- Projet sous GPL de Michael Poppitz  
<http://www.sump.org/projects/analyzer/>
- Matériel
  - Spartan-3 Starter Board (ou autres)
  - Conversion 5V -> 3.3V
  - Sondes

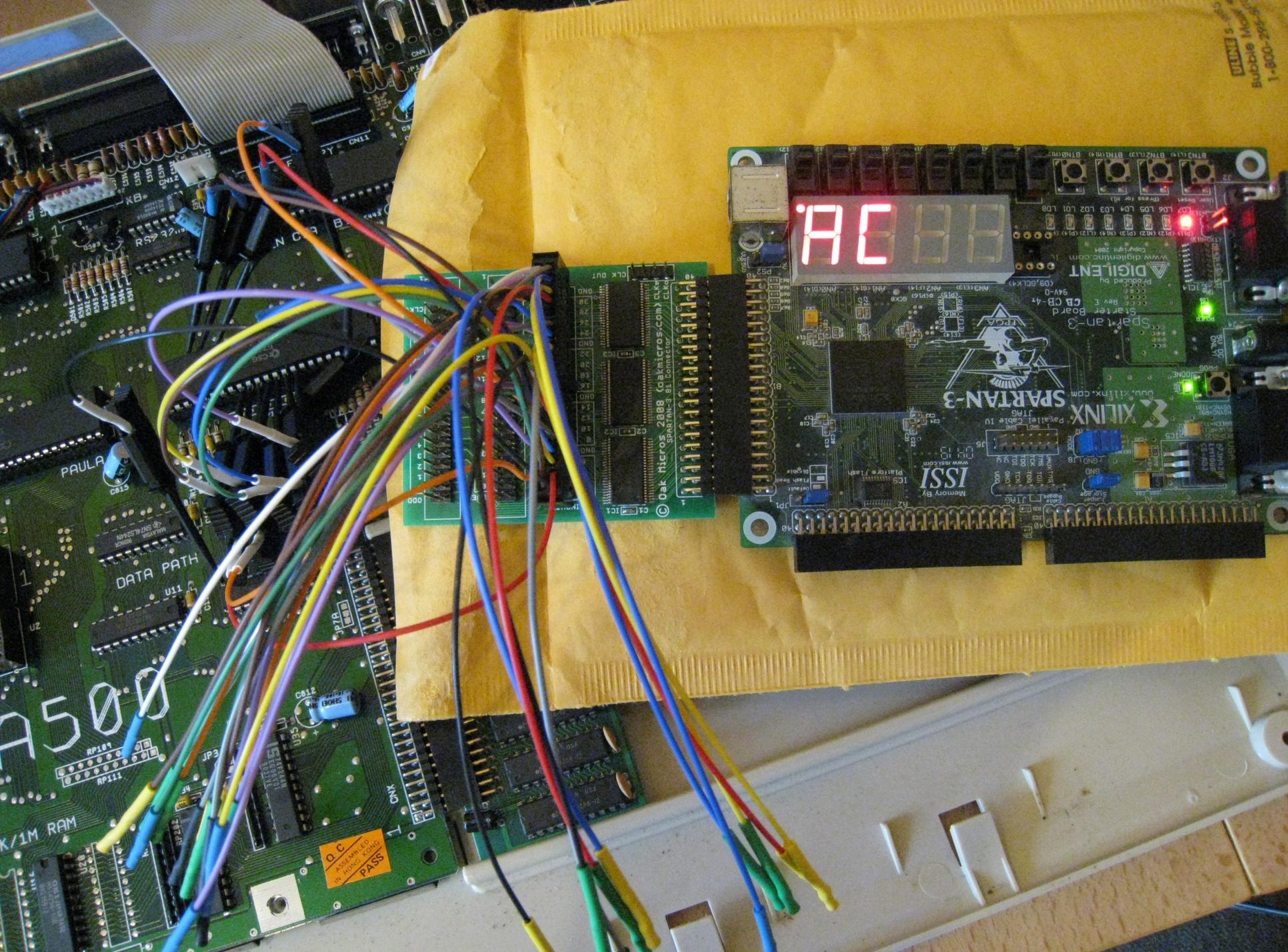


# SUMP LA - Caractéristiques

- 16 ou 32 voies
- 200 Mhz
- 256 Ksamples
- Triggers
  - Série
  - Parallèle
  - Simples ou complexes
- Logiciel open-source (GPL)







**XILINX**  
Spartan-3 Starter Board  
Rev E CB-47  
Produced by  
www.digilent.com  
Digilent

0000

Memory By  
**ISSI**  
Parallel Cable I/O  
J116

PS2

BTN3(L1-9) BTN2(L10) BTN1(M-4) BTN0(M1)

L06 L05 L04 L03 L02 L01 L00

Power Reset

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Spartan-3 81 Connector

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DATA PATH

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# Etude de l'Amiga 500

- Etude des accès mémoire
- GARY
  - Décodage « adresses hautes »
  - Arbitrage 68000
- FAT AGNUS
  - Décodage « adresses basses »
  - Contrôleur DRAM
  - Périphériques (Décodage, DMA)

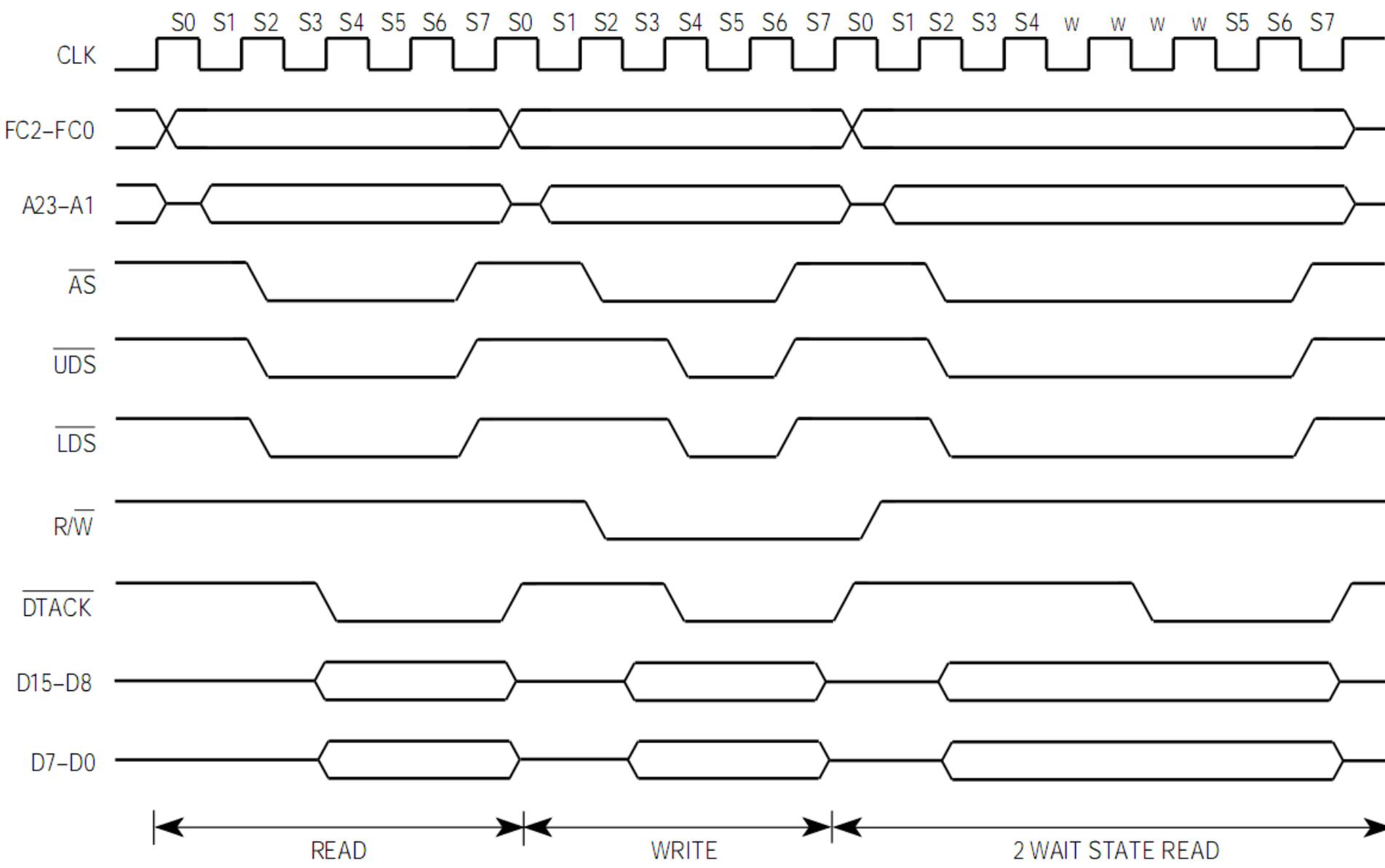
# Etude de l'Amiga 500

Analyse des schémas



# Etude de l'Amiga 500 - 68000

- ASn : Address Strobe
- RnW : Read / Write
- UDSn,LDSn : Upper,Lower Data Select
- VPAn : Valid Peripheral Address
- DTACKn : Data Transfer Acknowledge



**Figure 5-3. Read and Write-Cycle Timing Diagram**

# Etude de l'Amiga 500 - GARY

- OEBn : Enable bus write buffers
- OELn : Enable bus read latches output
- LATCHn : Enable bus read latches latch
- ROMENn : Enable ROM
- RAMENn : Enable RAM
- REGENn : Enable Amiga Registers

# Etude de l'Amiga 500 - AGNUS

- RAS0n,RAS1n : Row Address Selection
- CASLn, CASUn : Column Address Selection
- WEn : Read / Write
- DRA0..8 : DRAM Address
- RGA0..7 : Amiga Register Address Selection
- DMAL : DMA Request (PAULA)
- BLITn : Blitter (DMA) Request
- BLISSn : Blitter Slowdown

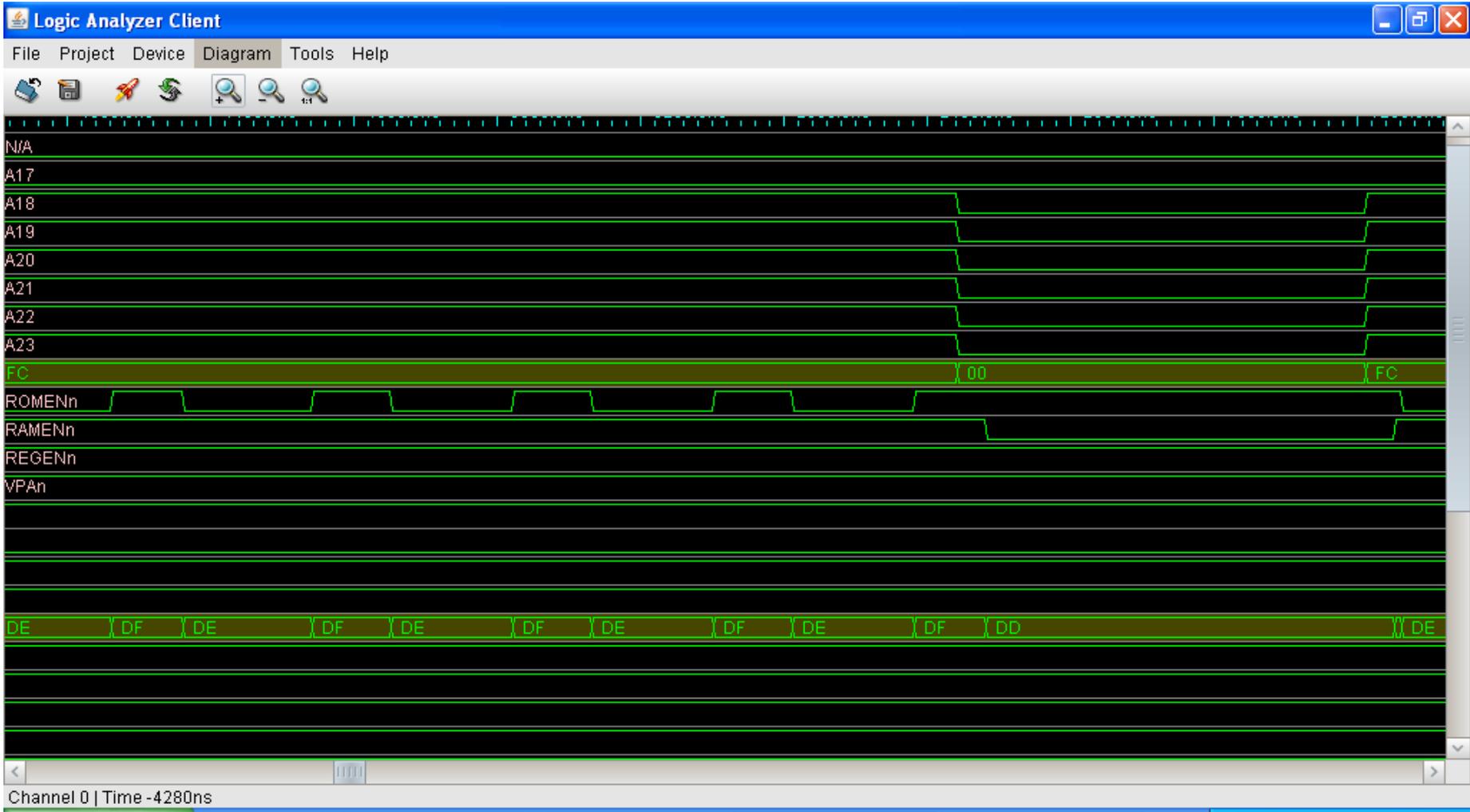
# Etude de l'Amiga 500

Décodage des Adresses  
(GARY)

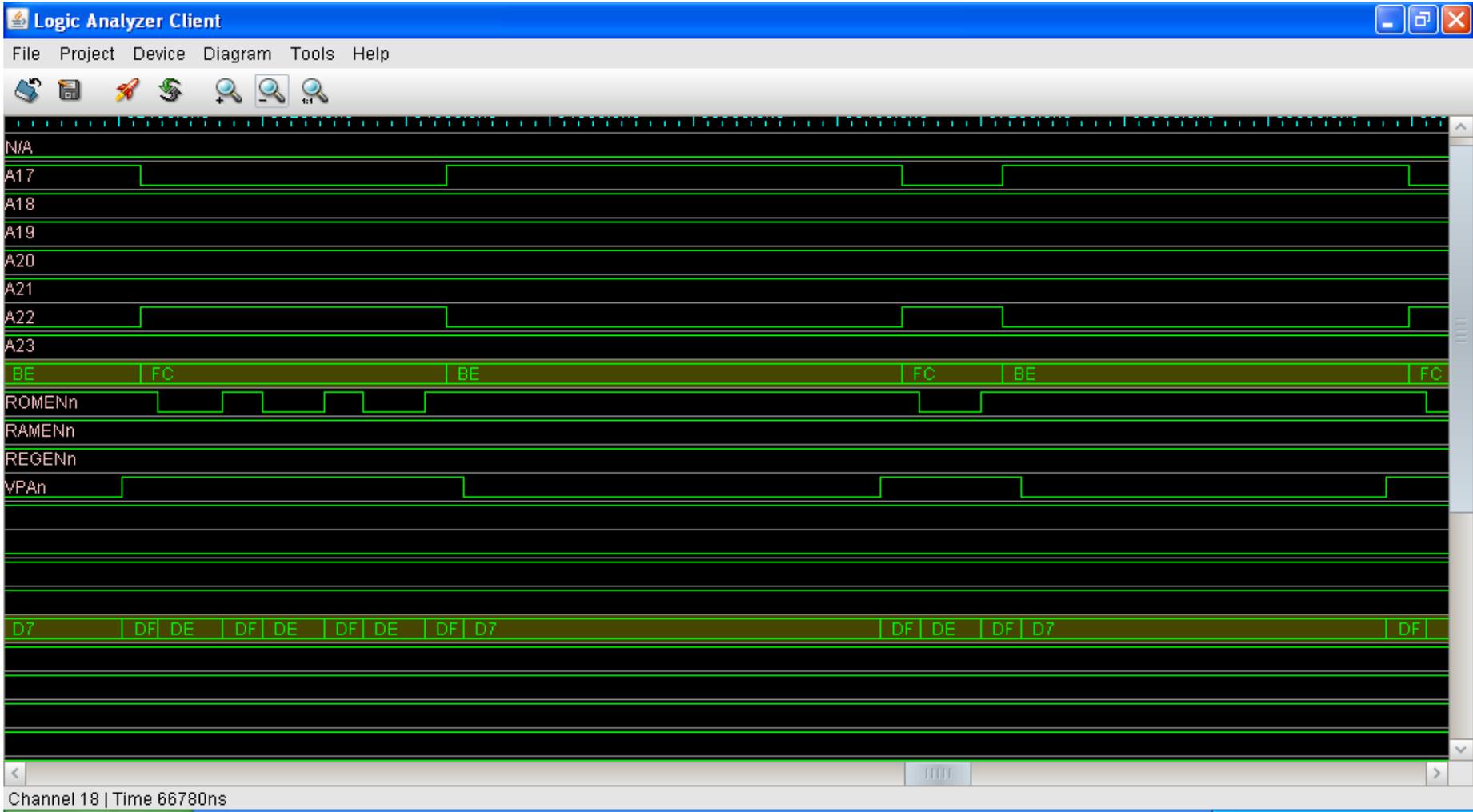
# Amiga Memory Map

Address	Size [KByte]	Description
0x0000 0000	256.0	Chip RAM
0x0004 0000	256.0	Chip RAM ( <a href="#">A1000</a> option card)
0x0008 0000	512.0	Chip RAM expansion
0x0010 0000	1024.0	Extended Chip RAM for <a href="#">ECS/AGA</a> .
0x0020 0000	8192.0	Primary auto-config space (Fast RAM)
0x00A0 0000	1984.0	Reserved
0x00BF D000	3.8	<a href="#">8520-B</a> (even-byte addresses)
0x00BF E001	3.8	<a href="#">8520-A</a> (odd-byte addresses)
0x00C0 0000	1536.0	Internal expansion memory (pseudo-fast, Slow RAM on Amiga 500)
0x00D8 0000	256.0	Reserved
0x00DC 0000	64.0	<a href="#">Real time clock</a>
0x00DD 0000	188.0	Reserved
0x00DF F000	4.0	Custom chip registers
0x00E0 0000	512.0	Reserved
0x00E8 0000	64.0	<a href="#">Zorro II</a> auto-config space (before relocation).
0x00E9 0000	448.0	Secondary auto-config space (usually 64K I/O boards)
0x00F0 0000	768.0	256K System ROM ( <a href="#">Kickstart</a> 1.4 or higher)
0x00FC 0000	256.0	256K System ROM

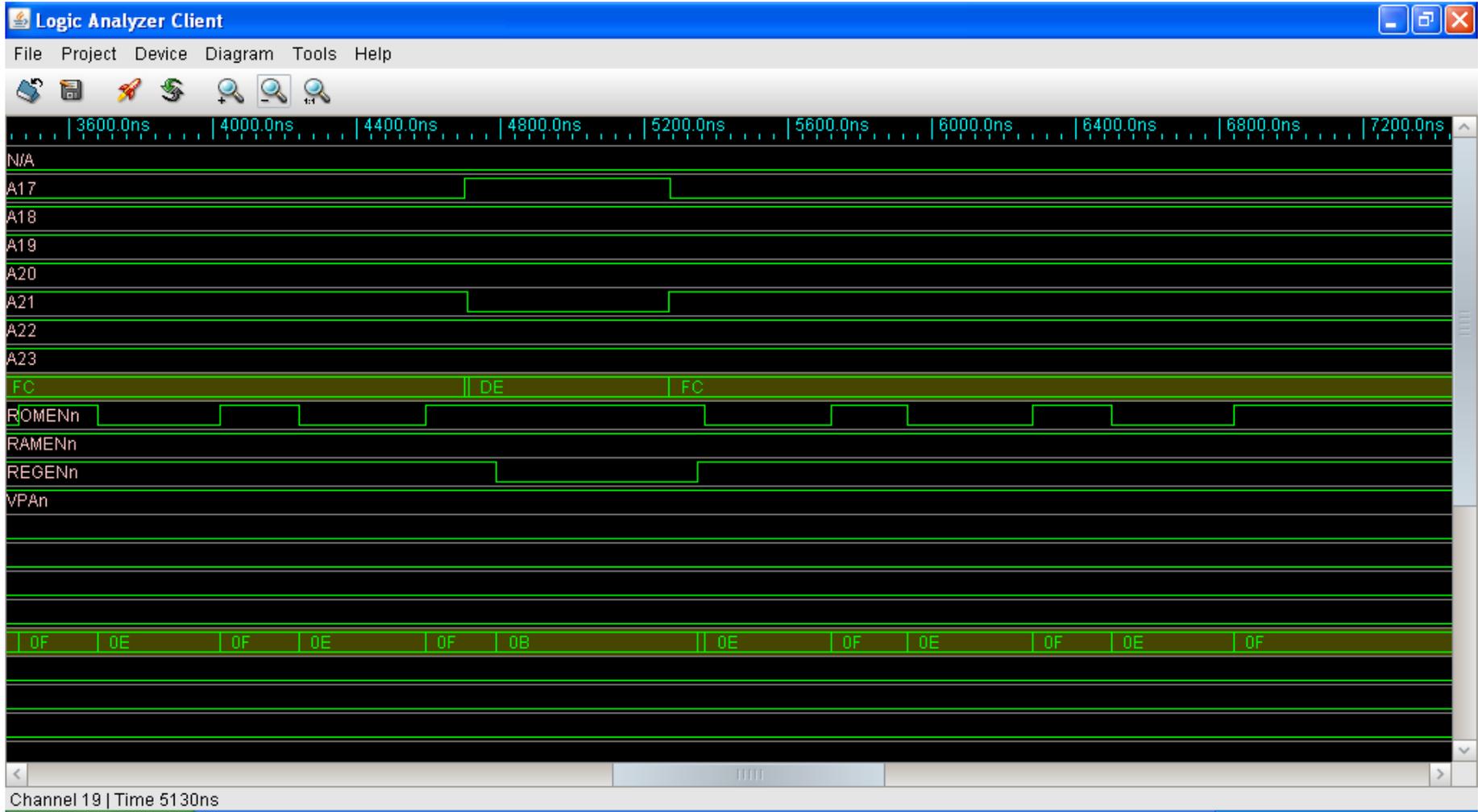
# ROM / RAM



# Périphériques (8520)



# Amiga Chipset



# Etude de l'Amiga 500

Accès mémoire  
(GARY / AGNUS)

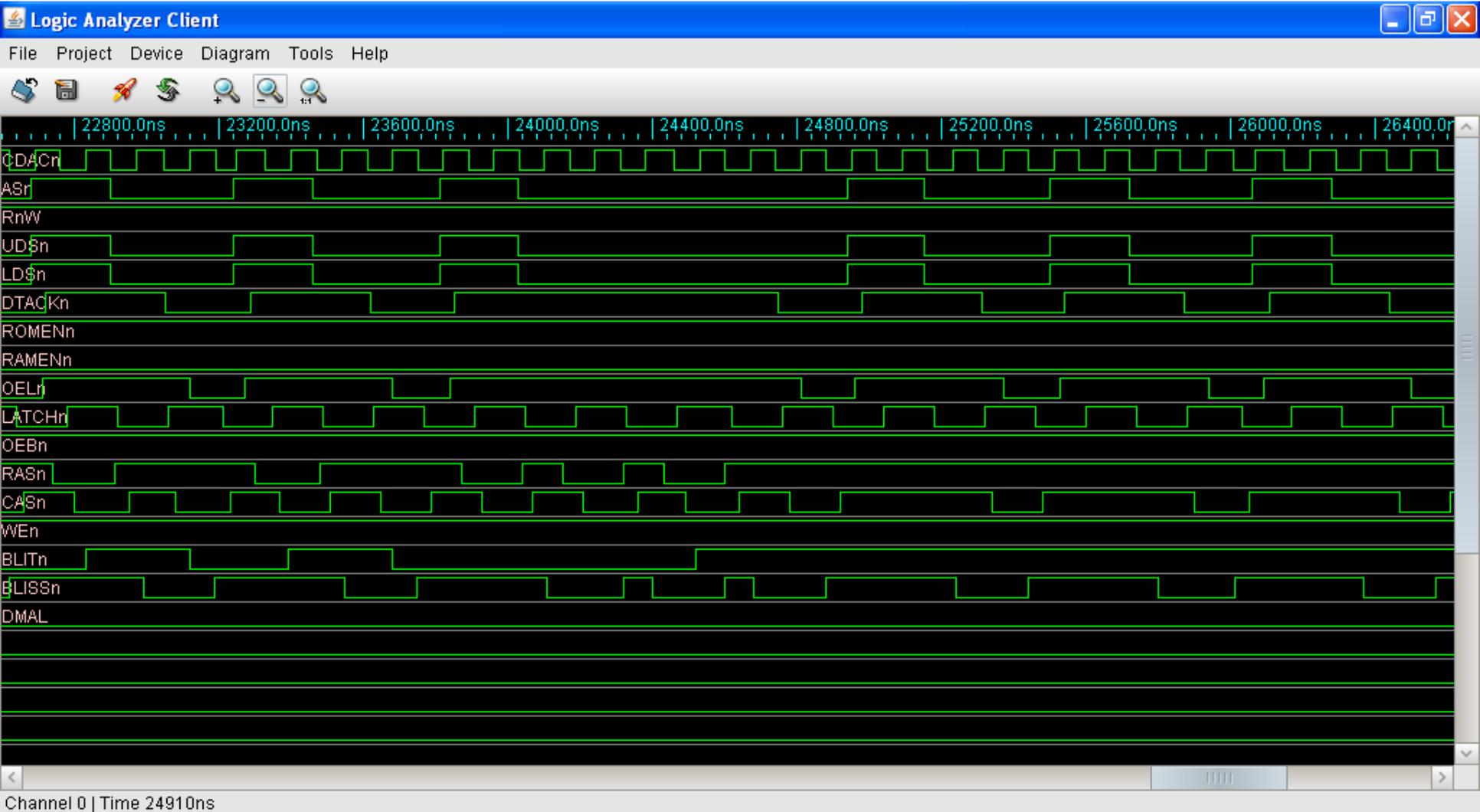
# Accès ROM / RAM (lecture)



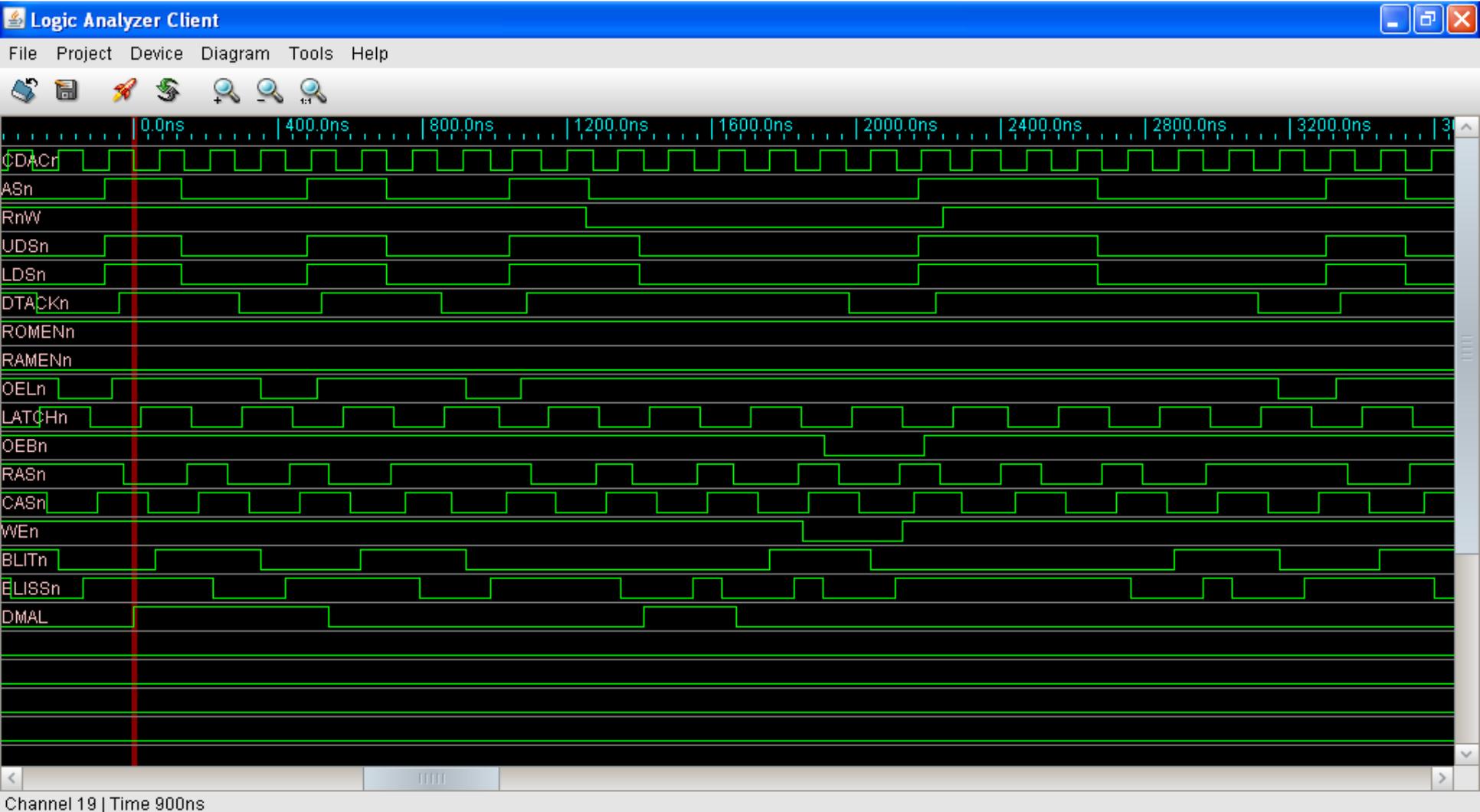
# Accès RAM (écriture)



# DMA (AGNUS)



# DMA (PAULA)



# Questions / Réponses